A Rail-To-Rail Cmos Buffer Amplifier with Low Power Leakage for Flate Panel Displays

Sadhana Sharma and Shyam Akashe

Abstract— A rail-to-rail high speed buffer amplifier is proposed with power gating technique, which is used for flat panel displays. By using power gating technique buffer amplifier has achieved the reduced leakage power by more than two orders of magnitude. The presented buffer amplifier is the combination of two transconductance amplifiers, two current comparators, A push-pull output stage and two sleep transistors. The buffer amplifier is simulated at the 45nm technology with cadence software at 3v supply voltage. The leakage current of this circuit is reduced by 4% (i.e. .79×10-6µA). The settling time for a rail-to-rail buffer swing is settled down to the range of .299×10-6µA.

Index Terms— Rail-to-rail buffer, Low power gating transistors, Transconductance amplifiers, Current comparators, Leakage power, Liquid crystal displays, Power gating technique.

1 INTRODUCTION

To increase the display resolution, the load capacitance of the buffer amplifier is also increased, while the settling time is reduced. As we know the inbuilt buffer amplifier produce the power dissipation at high level. To achieve the high resolution, low power dissipation and high driving capability column drivers are mostly used by Chi and Ping et al. [1].The analysis of analog circuit is very difficult, when we design the column drivers especially for LCDs. In this case buffer amplifier plays an important role, because they determine the speed, resolution, voltage swing, transient response and the power dissipation of column drivers by Chien and Jia et al.[2]. Two stage OTAs with unity gain configuration is mostly applied in LCD output buffers. Two-stage amplifiers consists the additional circuitry of current comparator to improve the large signal performance, here current comparators are used to enhance the slew rate of output amplifier by David and Gaetano et al.[3].

A low dropout linear regulator (LDOs) is also designed which dissipates the low static power and the transient response of this circuit is also good without transient overshoot when driving large capacitive loads used by Ka Nang and Yuen sum [4].This paper was realized by a new current efficient analog driver for CMOS LDO. To improve the transient response, the concept of the LDO with the current boosting buffer was presented by Massimo and Gaetano [5] , [6].In the paper of D.J.R Crystaldi and S.Pennis et.al.[7]. A high driving capability CMOS buffer amplifier for TFT-LCD source drivers is performed which contains a pair of auxiliary driving transistors. It contains the comparators with the basic differential amplifiers to reduce the power dissipation.

A compact low-power rail-to-rail buffer is performed for large size LCD applications .It performs the high slew rate by applying the push- pull output buffer with two complementary type input amplifiers give a dual-path push-pull operation of the output buffer. An auxiliary biasing network is used to control the output quiescent current without increase the power dissipation was used by Wang and Qui et.al.[8],[9],[10]. Liquid crystal displays are mostly used for flat panel displays. The applications of LCDs include cellular phones, personal digital assistants, notebooks, monitors and digital TVs. To achieve the desired color depth and resolution for flat panel displays, we need a driver circuit, which is included by the LCDs. Column driver plays an important role for the high quality display. A column driver circuit includes the shift registers, input resisters, data latches, level shifters, digital to analog converters (DACs) and output buffers was presented by Jong and Dong et al.[11]. A rail-to-rail buffer amplifier gives low power and high speed response with improved current summing circuit was proposed. This current summing circuit includes two comparators that was achieved the switching of output stages without extra area and power was presented by Jun and Zheng et.al. [12].

A class-AB rail-to-rail CMOS buffer amplifier with complementary folded-cascode input, high CMRR was proposed by Yen and Fang [13].To achieve the good power efficiency a class-B CMOS output buffer is proposed, it contains the nonlinear elements like comparators to reduce the size of the output stage performed by Pang and Jiin [14]. Another class-B buffer is presented to achieve the low power and rail-to-rail swing by using dc level shifting current mirror. This type of class-B buffer is used for every size of high quality display panel applications with the fast settling time over the large capacitive load was presented by Wein and Shigeisa et.al.[15]. To reduce the offset voltage of output class-B buffer with offset compensation circuit is proposed, which gives the high resolution applications performed by Ming-Dou and Chi-Kang et.al.[16]. A rail-to-rail buffer amplifier with high slew rate

presented for flat panel displays, which is based on phase compensation technique to improve the phase margin. This circuit consist the two transconductance amplifier with two current comparators was presented by Merin and Shahram et.al.[17].

To drive the very high capacitive loads buffer amplifiers are mostly used in analog and mixed mode integrated circuits. In this paper a new rail-to-rail buffer amplifier with low leakage current, low settling time and reduced delay is proposed, which is useful for LCDs applications. The working of this circuit is based on the reference [16]. This circuit also consist the two transconductance amplifiers, two current comparators, output stage and additional sleep transistors are also connected at VDD and VSS. These additional transistors are mainly used to reduce the leakage current of the circuit in standby mode.

2 MAIN FEATURES OF RAIL TO RAIL BUFFER AMPLIFIER

2.1 Rail-to-rail swing

To achieve the rail-to-rail swing, an NMOS pair and an PMOS pair added in parallel configuration [11].The CMR voltage range of the n-channel pair is written as;

$$V_{cmn} \geq V_{ss} + V_{gsn} + V_{dsn} \quad (1)$$

Where V_{gsn} and V_{dsn} are the gate-source voltage and drain-source voltage respectively. Similarly, the CMR of p-channel pair is written as;

$$V_{cmp} \leq V_{dd} + V_{gsp} + V_{dsp} \quad (2)$$

To get rail-to-rail input range, one or both pair should be in "active mode", which requires

$$V_{cmp-max} \geq V_{cmn-min} \quad (3)$$

Put the equation (1) and (2) in equation (3)

$$V_{dd} - V_{ss} \geq V_{gsp} + V_{dsp} + V_{gsn} + V_{dsn} \geq 2V_{th} \quad (4)$$

Here equation (4) shows that V_{th} of NMOS and PMOS are same, and then the value of applied voltage should be higher than twice of the threshold voltage V_{th} of the applied technology.

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2.2 Power dissipation of circuit

The maximum power allowed to dissipate in a circuit is defined as,

$$P_d = \frac{(T_{jcmax} - T_a)}{\theta_{ja}} \quad (5)$$

Where P_d is the power dissipation, T_{jcmax} is the maximum junction temperature [13]. T_a is ambient temperature. **Θja is the** thermal resistance; depends on parameters such as die size, package size and package material. The smaller will be the die size and package, the higher θ_{ja} is becomes then the power dissipation will be reduced .Total power dissipation in a device can be calculated as,

$$P_d = P_q + P_o \quad (6)$$

P_d is the quiescent power dissipated in a circuit with no load connected at the output. P_o is the power dissipated in the circuit with a load connected at the output, this power cannot be dissipated by the load.

P_d = supply current × total supply voltage with no load.

P_o =output current × voltage difference between supply voltage and output voltage of the same supply.

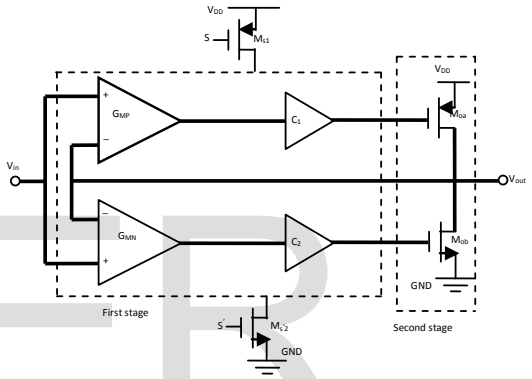
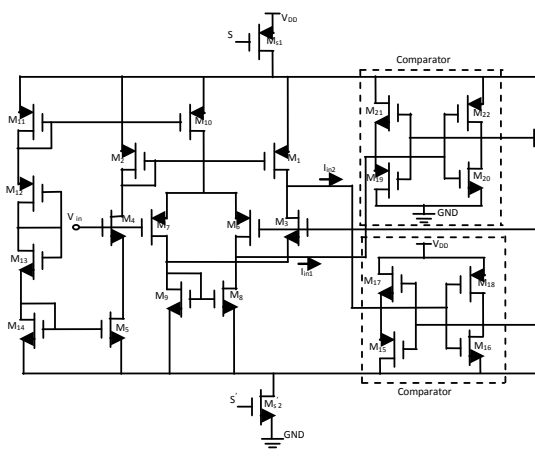


Fig.1. Shows the block diagram of proposed buffer amplifier.



. Fig.2.circuit diagram of proposed buffer amplifier.

3 PROPOSED BUFFER AMPLIFIER

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which can be divided into three parts, the first part is the first stage, which is consisting two basic structures of transconductance amplifier GMP-GMN and comparators C1-C2. The second stage is consisting push-pull output transistors Moa-Mob and the third part is made up of two sleep transistors Ms1-Ms,2 . This circuit gives the function of buffer amplifier with the low leakage power. This circuit is based on the power gating technique, which reduces the leakage power of the cir cuit in the standby mode. Proposed buffer amplifier contains the common source output stage which gives the high gain and full swing of the wave. Here the output of the proposed buffer amplifier is designed especially for VDD or 0V. From this line we can conclude that when transistor Mo2 will come in on condition, then VDD will be pulled down by the output voltage. After that when the Mo1 will on, and then 0V will be pulled by the output voltage.

The circuit diagram of designated proposed buffer amplifier is shown in fig. (2). Consisting input of this circuit is divided into two parts inverting and non-inverting type. Here the inverting input of the circuit is connected with output voltage. And the non-inverting terminal of the circuit is connected with the input signal by help of this phenomenon we have achieved a unity gain buffer amplifier. This circuit has biasing transistors M11-M14. Transistor biasing is an important function for any electronics circuit. In the transistor biasing the amount of voltage and current is controlled that is used to achieve desired amplification and switching characteristics of the transistor.

As shown in fig. (2) , transconductance amplifiers are made up of NMOS and PMOS input differential pairs, which can be implemented by the source coupled differential pairs M3-M4 and M6-M7 respectively, this phenomenon gives the rail-to-rail capability. These differential pairs are got the DC biasing currents by help of the transistors M5-M10. The transistors M15-M18 and M19-M22 are used to provide the function of the current comparators. Current comparators are used to improve the capability of finding the source current at the high impedance node. Current comparators are basically used for the nonlinear current mode signal processing and analog to digital converters [18]. As we know that the buffer circuit gives output voltage same as input voltage. In this circuit bias current I is divided into equal two parts I/2, which is supplied by the transistors M5 (M10). The current I/2 will flow through transistors M6 (M3) and M7 (M4). The drain voltage of M9 (M2) is same as the drain voltage of M8 (M1), because of the same values of the (W/L) 9 = (W/L) 8 and (W/L) 2= (W/L) 1, here channel length modulation is neglected.

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4 THEORY OF APPLIED TECHNIQUE

In the power gating technique one PMOS is connected at the VDD node of the circuit and one NMOS is connected at the GND node of the circuit. In the active mode of the circuit the sleep transistor is on and the functionality of the circuit is as usual and in the standby mode, the switch transistor is turned off, so the whole circuit is disconnected from the ground or power. In this circuit, the supply voltage is turned off during the standby mode by using a PMOS transistor or an NMOS transistor. By help of this technique this circuit has got the

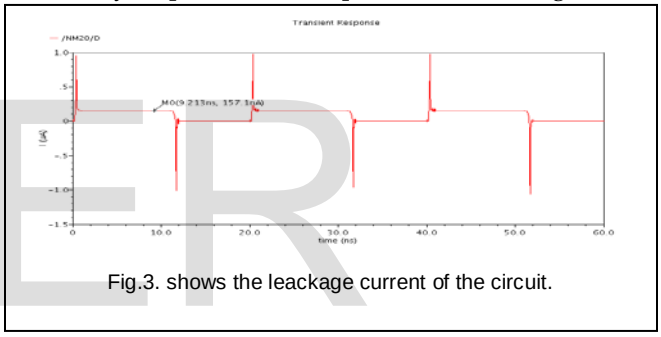

Fig.3. shows the leackage current of the circuit.

reduced leakage current of the power gated logic transistor, where the body effect is increased. This technique reduces the leakage power more than two orders of the magnitude of the circuit.). This reduced leakage current gives the reduced lea

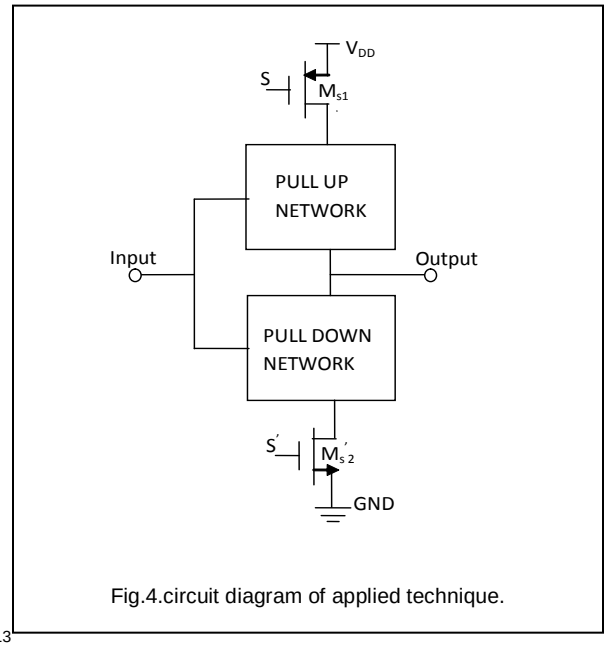

Fig.4.circuit diagram of applied technique.

kage power as shown in figure (3) and (4) respectively.

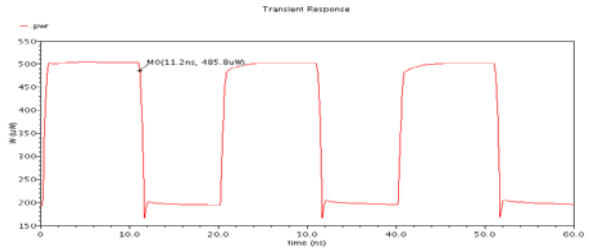

Fig. 5.Shows the input-output waveform in the form of square wave pattern of circuit..

5 Simulation Results

To realize the advantages of the given class-B buffer amplifier over the reference class-B amplifier [17], simulations have been performed with virtuoso tool by help of the CADENCE software at 45 nanometer technology. Table I gives the achieved results of the proposed buffer amplifier. This circuit gives the simulation results at 3V supply voltage. Here figure (2) has the circuit diagram which has the simulation results with the transient response and dc response. The transient response of the circuit is achieved with input-output square waveform is given in figure (6) with the 600pF capacitive load. This simulation is performed in the 12µs. Another transient response is given with the input-output saw tooth waveform is given in figure (7) with the 1nF capacitive load. After it, by help of the power gating technique leakage current is reduced which is shown with the dc response figure (8).

TABLE 1
Simulation Results

Parameters	Simulation results
Leakage power (µw)	485.5×10^{-6}
Leakage current (nA)	157.1×10^{-9}
Slew rate (V/µs)	15.7×10^{-6}
Bandwidth (db)	6.58×10^{-6}
Delay (µs)	-7.702×10^{-6}
Settling time (µs)	$.299\times10^{-6}$
Spectral power (mw)	3.49×10^{-3}
Rise time (ns)	100.2×10^{-9}

6 Conclusion

In this paper a Class-B buffer is proposed with the reduced leakage technique i.e. power gating technique. From the above theory we can conclude that this technique is useful for electronic systems under the standby mode. Here we have achieved the dc and ac responses with different leakages. Mainly leakage power is reduced 10% in the comparision of reference [17]. From the table -1 we can conclude abo-

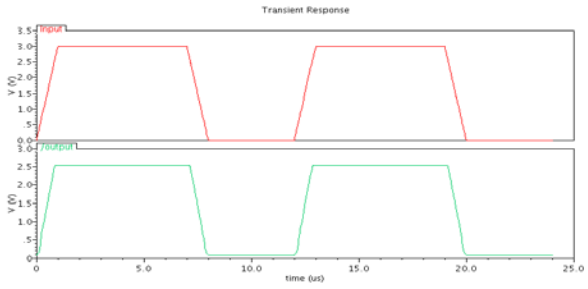

Fig. 6.Shows the input-output waveform in the form of square wave pattern of circuit..

ut this paper, that it has achieved the values of parameter at good level. The slew rate of this circuit is enhanced by 4% (i.e. 15.7×10-6V/µs). The settling time is also reduced by the 2% (i.e. .299×10-6 µs). Now we can say that by reducing the settling time, the speed of the circuit is increased. This circuit is faster than reference circuit. This circuit consumes lowest delay.

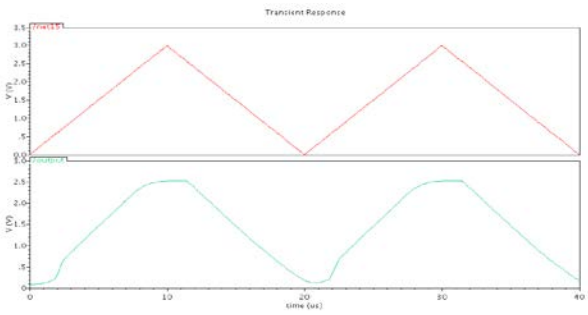

Fig. 7. Shows the input-output waveform in the sawtooth pattern of the circuit.

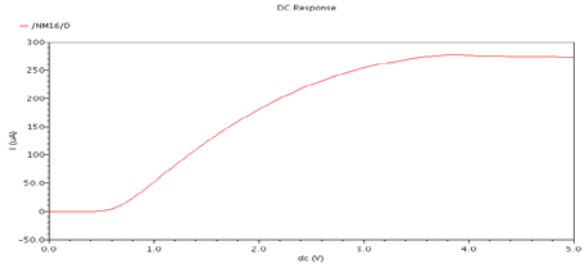

Fig. 8. Shows the DC response of the circuit

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